Amendment to the Claims:

The claims under examination in this application, including their current status and changes made in this paper, are respectfully presented.

1 (canceled).

2 (canceled).

3 (previously presented). A digital system comprising:

at least a first processor having an address space;

a local memory connected to the first processor and occupying a portion of the address space of the processor, the local memory operable to respond to transfer requests from the first processor, the local memory comprising a data array arranged as a plurality of segments and a plurality of valid bits operable to indicate that a corresponding segment contains valid data, wherein each of the plurality of segments has a corresponding indicator bit within the plurality of valid bits; and

direct memory access (DMA) circuitry connected to the local memory, the DMA circuitry operable to transfer data to a selectable portion of segments of the plurality of segments from a selectable region of a second memory and operable to set, to a valid state, a selected portion of valid bits of the plurality of valid bits corresponding to the selectable portion of segments; and

miss detection circuitry connected to the plurality of valid bits, the miss detection circuitry having a miss signal for indicating when a miss is detected in response to a request from the first processor to a first segment;

wherein the processor stalls in response to the miss signal until the DMA circuitry sets a first valid bit corresponding to the first segment to a valid state.

4 (original). The digital system of Claim 3, further comprising timeout circuitry connected in a responsive manner to the miss signal having an output connected to an interrupt

input of the first processor, whereby the timeout circuit is operable to interrupt the processor if the DMA circuitry does not validate the first segment within a certain period of time.

5 (previously presented). The digital system of Claim 3, further comprising:

address circuitry responsively connected to the miss signal, the address circuitry operable to transfer data to the first segment in response to the miss signal.

6 (original). The digital system of Claim 5, wherein the DMA circuitry is operable to transfer a block of data to the selected portion of segments in such a manner that a transfer to the first segment holding valid data within the selected portion of segments is inhibited.

7 (currently amended). A digital system, comprising:

at least a first processor having an address space;

a local memory connected to the first processor and occupying a portion of the address space of the processor, the local memory operable to respond to transfer requests from the first processor, the local memory comprising a data array arranged as a plurality of segments and a plurality of dirty bits operable to indicate that a corresponding segment contains dirty data, wherein each of the plurality of segments has a corresponding dirty bit within the plurality of dirty bits; and

direct memory access (DMA) circuitry connected to the local memory, the DMA circuitry operable to transfer data to a selectable portion of segments of the plurality of segments from a selectable region of a second memory and operable to set, to a ~~valid~~ dirty state, a selected portion of dirty bits of the plurality of dirty bits corresponding to the selectable portion of segments.

8 (original). The digital system of Claim 7, wherein the DMA circuitry is operable to transfer data from a selectable portion of segments to a selectable region of the second memory in accordance with a corresponding portion of dirty bits, such that only segments within the selectable portion of segments whose corresponding dirty bit is in a dirty state are transferred.

9 (previously presented). The digital system of Claim 8, wherein a first dirty bit is operable to be set to a dirty state in response to a write transaction by the first processor to a first segment associated with the first dirty bit, and

wherein the first dirty bit is operable to be reset in response to a write transaction by the DMA circuitry to the first segment associated with the first dirty bit.

10 (original). The digital system of Claim 9, further comprising a first mode circuit connected to DMA circuitry, wherein the DMA circuitry is operable to transfer a block of segments from the local memory to the second memory in a manner that only segments within the block marked as dirty are transferred when the first mode circuit is in a first state, and wherein the DMA circuitry is operable ignore the plurality of dirty bits such that the entire block is transferred when the first mode circuit is in a second state.

11 (previously presented). The digital system according to Claim 3 being a cellular telephone, further comprising:

an integrated keyboard connected to the CPU via a keyboard adapter;

a display, connected to the CPU via a display adapter;

radio frequency (RF) circuitry connected to the CPU; and

an aerial connected to the RF circuitry.

12 (canceled).

13 (canceled).

14 (previously presented). A method of operating a digital system having a processor and a local memory that occupies a portion of an address space of the processor, comprising the steps of:

organizing the local memory as a plurality of segments;

associating a plurality of indicator bits with the plurality of segments such that each segment has at least one corresponding indicator bit; and

setting a selected portion of indicator bits associated with and corresponding to a selected portion of segments in the local memory to a valid state in response to a direct memory

access (DMA) transfer of a first data value from a selectable location in a second memory to the first location segment in the local memory;

detecting a miss when a requested segment is indicated as invalid in response to a request from the first processor to a first segment; and

stalling the processor in response to the detected miss until the DMA transfer sets a first valid bit corresponding to the first segment to a valid state.

15 (previously presented). The method of Claim 14, further comprising the step of interrupting the processor if the DMA transfer does not validate the first segment within a certain period of time.

16 (previously presented). The method of Claim 14, wherein the step of stalling stalls the processor until a block of data is transferred to the selected portion of segments.

17 (previously presented). The method of Claim 14, further comprising:

then writing, with the processor, data to a selected segment of the local memory;

associating a plurality of dirty bits with each of the plurality of segments of the local memory; and

responsive to the writing step, setting the dirty bit of the selected segment to indicate that the selected segment contains modified data.

18 (previously presented). The method of Claim 17, further comprising the step of transferring data from a selected portion of segments to a selected region of the second memory in accordance with a corresponding portion of set dirty bits, such that only segments within the selected portion of segments whose corresponding dirty bit is in a set state are transferred.

19 (previously presented). The method of Claim 18, further comprising the steps of

after the step of transferring data from a selected portion of segments to a selected region of the second memory in accordance with a corresponding portion of set dirty bits, transferring new data into at least one segment of the selected portion of segments by DMA transfer; and

resetting the dirty bit associated with the at least one segment in response to the step of transferring new data.

20 (previously presented). The method of Claim 17, further comprising the steps of:

setting a fill mode to a selected state; and

transferring a block of segments from the local memory to the second memory in a manner that either only segments within the block having their associated dirty bits set are transferred when the fill mode is in a first state, or all segments of the block of segments are transferred regardless of the associated dirty bits when the fill mode is in a second state.

Claims 21 and 22 are canceled.